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EVALUATION OF A HIGH POWER INVERTER FOR POTENTIAL SPACE APPLICATIONS

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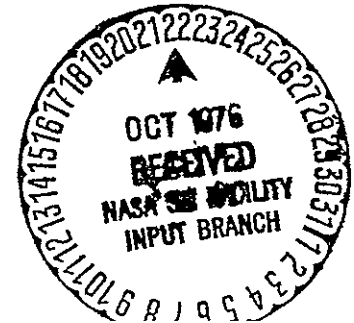
August 1976

NASA

George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama



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16 ABSTRACT

The ADM-006 inverter discussed in this report utilizes a unique method of using power switching circuits to produce three-phase low harmonic content voltages without any significant filtering. This method, developed by Delco Electronics of General Motors Corporation, is referred to as the "Power Center" approach to inverter design and is explained briefly in this report.

This report presents the results of tests performed by MSFC to evaluate Delco's claims on inverter performance, especially when required to provide power to nonlinear loads such as half or full wave rectified loads with capacitive filtering. Test procedures and results are described.

These tests show that the Power Center inverter essentially met or exceeded all of Delco's claims excluding voltage regulation (3.9 percent versus specified 3.3 percent) and would be a good candidate for high power inverter applications such as may be found on Space Station, Spacelab, etc.

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DEFINITION OF SYMBOLS

Symbol	Definition
Adc	Amperes direct current
A rms	Amperes root mean square
I	Current
kVA	Kilovolt amperes
kVAR	Kilovolt amperes reactive
kW	Kilowatt
N	Neutral
η	Inverter efficiency
PF	Power factor
V	Voltage
Vdc	Voltage direct current
V_{L-N}	Voltage line to neutral
V trms	Voltage true root mean square
THD	Total harmonic distortion

TECHNICAL MEMORANDUM X-73341

EVALUATION OF A HIGH POWER INVERTER FOR POTENTIAL SPACE APPLICATIONS

INTRODUCTION

The ADM-006 inverter evaluated in this test program (Fig. 1) utilizes a unique method of using power switching circuits to produce three-phase low harmonic content voltages for possible future high power inverter applications such as may be found on Space Station, Spacelab, etc. This method, developed by Delco Electronics Division of General Motors Corporation, is referred to as the "Power Center" approach to inverter design.

The primary purpose of this test program was to evaluate Delco's claims on inverter performance (Appendix A), especially when supplying non-linear or transient loads, and evaluate the inverter as a possible candidate for future high power inverter applications. A secondary benefit of this program was to familiarize MSFC personnel with characteristics of the Power Center approach employed in the ADM-006 inverter.

ADM-006 INVERTER CIRCUIT DESCRIPTION

The complete power circuit for the three-phase inverter consists of left, center, and right circuits, each generating corresponding segments of an approximation of a sine wave without filtering. The inverter consists of a power center which is a three-phase thyristor bridge circuit, a step-former which is a tapped autotransformer with the necessary thyristor and transistor switches for step selection, a diode-thyristor circuit that energizes the autotransformer for "left" and "right" circuit operation, and a set of thyristors called phase selectors that connect the left and right step voltages to the three phase output lines in the proper sequence. The center circuit handles more than 80 percent of the power at approximately 99 percent efficiency. This is the basis for the name

Power Center. The remaining 20 percent of the power passes through the less efficient autotransformer and associated circuitry. This circuitry, although handling only a small portion of the total power, provides a significant contribution to the low distortion sine-wave output.

TEST PROCEDURES AND RESULTS

The ADM-006 inverter was tested in accordance with MSFC test procedure 40M22460 which is included in Appendix B of this report. Procedures are specified in 40M22460 for performing the following tests: (a) rated power output tests, (b) rated output voltage tests, (c) power factor and waveform tests, (d) low input voltage tests, and (e) rectifier load tests.

A photograph of the typical laboratory test setup is presented in Figure 2.

Rated Output Power Tests

The inverter performed satisfactorily when delivering balanced and unbalanced three-phase loads continuous and up to a 28.6 kW load (short term overload rating is 25 kVA) for 1 min. Test results are shown in Table 1. Maximum power delivered to the load was 21.2 kW and not 24 kW as specified in the test procedure. The difference in loading can be attributed to the fact that the load bank used was calibrated to deliver rated power (per switch and vernier control settings) at input voltages of 120 V. However, the inverter was run at loads up to 28.6 kVA (4.62 kW resistive and 8.0 kVAR inductive per phase on load bank dial settings) for periods of approximately 2 min in an unspecified overload test. The inverter automatically shuts itself down when thermal limitations are exceeded, and the inverter did successfully shut down during operation of this overloaded condition.

Inverter efficiency versus resistive and inductive loads are plotted in Figure 3.

Rated Output Voltage Test

These tests were conducted to determine inverter regulation and distortion when operating at rated load. Voltage regulation in percent is defined by

$$\frac{V_{\text{No Load}} - V_{\text{Full Load}}}{V_{\text{Full Load}}} \times 100$$

Using this formula and the data in Table 2, regulation is determined to be 3.9 percent which is slightly higher than the 3.3 percent quoted by Delco. Output voltage is plotted versus load current in Figure 4. Total harmonic distortion was measured and found to be no worse than 3.2 percent for purely resistive three-phase loads (Fig. 5).

Power Factor and Waveform Tests

These tests were performed to determine the inverter's reaction to inductive or capacitive loads of varying power factors. Data from these tests are shown in Tables 3 and 4. Graphical interpretation of the data is shown in Figures 6 through 9. The highest total harmonic distortion measured occurred during inductive loading and was within Delco's specified 4 percent (measured 3.6 percent as shown in Table 3 and Fig. 7). A review of the data supports the claim that the Delco Power Center inverter (ADM-006) is relatively insensitive to capacitive and inductive loads (reactive). Inverter efficiency drops as reactive loading is increased (Figs. 6 and 9). Note also that harmonic distortion increases with increased reactive loading. The increased harmonic content produced by the reactive loading results in increased losses (and decreased efficiency) in the inverter primarily because the power center with just two semiconductor junction voltage drops and a 99 percent efficiency is handling a smaller percentage of the total current. Because of the reactive loads (current lagging or leading voltage), power that was handled by the power center now is channeled through the autotransformer and left or right circuits by the step/phase selectors. Power flowing through this path encounters 11 semiconductor junction voltage drops which is 9 junctions more than encountered when traveling through the power center route. Figures 10 through 14 show inverter waveforms for the different types of loads.

Low Input Voltage Test

A test was conducted to verify that the inverter would operate satisfactorily at input voltages as low as ±90 Vdc. Data were also taken of input voltages of ±115 Vdc and the results from both tests are shown in Table 5.

The inverter provided three-phase balanced power of 15 kVA at power factors of 1.0 and 0.6. Data accumulated here and in Table 3 were used to plot the curves shown in Figure 9. Since there is no output voltage regulation on the ADM-006, output voltage phase to neutral varies directly with the input voltage. Hence, inverter efficiency decreases as the output voltage decreases, as shown in Figure 9. The decrease in efficiency can be attributed to the increasing significance of semiconductor junction voltage drops and other constant losses in the inverter as the power being processed is decreased

Rectifier Load Tests

The purpose of these tests was to determine if the ADM-006 would deliver undistorted power to nonlinear loads such as full or half wave rectified bridges with filter capacitors. Tests were generally performed as indicated in Procedure 40M22460; however, some changes had to be made to preclude blowing fuses in the inverter. The large initial surge of current required to charge the bank of capacitors in the filter would repeatedly blow fuses in the inverter because of the inverters overload current sense and crowbar protection scheme. Therefore, to run these tests, the capacitors first had to be charged up to their ultimate working dc voltage level (V_{out} in Table 6) which was done with an external power supply. This voltage, for the half wave rectified, is approximately 1.4 times the inverter's line to neutral voltage and for the full wave rectified is approximately 1.4 times the inverters line to line voltage. Data for these tests are shown in Table 6. Figures 15 through 18 show inverter output voltage and current wave forms as various nonlinear loads are applied. The ADM-006 can be seen to deliver power to nonlinear loads with very little increased distortion (1 percent higher than the Delco specified 4 percent). A more realistic and less severe test would have been performed with a more typical LC filter. Startup problems would have been eliminated and distortion would have been even less as demonstrated by an unscheduled test.

CONCLUSIONS

These tests show that the ADM-006 Power Center Inverter essentially met or exceeded all of Delco's claims excluding voltage regulation (3.9 versus 3.3 percent) and would be a good candidate for future high power inverter applications such as may be found on Space Station, Spacelab, etc.

Numerous small unexplained problems were encountered during operation of the inverter, i.e , frequent shutdown of the inverter by blown fuses or a tripped circuit breaker These nuisance shutdowns were attributed to noise in the automatic protection circuits.

Replacement of all integrated circuit devices in these circuits with CMOS or high noise resistant devices would have prevented most, if not all, of the problems encountered during testing Space applications of this type of inverter should incorporate this change

TABLE 1. RATED OUTPUT POWER TESTS

I	II 2 h minimum	III 2 h minimum	IV 1 min	V 1 min
Phase A	5	5	8	8
Phase B	5	5	8	8
Phase C (kW Setting)	5	2	8	4
V_+ to Com	+142	+142	+142	+142
V_- to Com (Vdc)	-142	-142	-142	-142
I_{IN} (+)	55.3	+45.3	78.8	65.8
I_{IN} (-) (Adc)	-56.2	-46.2	-79.7	-66.6
V_{A-N}	114.68	114.01	113.47	112.65
V_{B-N}	114.67	114.11	113.21	112.55
V_{C-N} (V trms)	115.14	118.39	113.81	117.88
I_A	43.49	43.12	61.45	60.76
I_B	43.62	43.5	62.09	61.76
I_C	43.5	20.23	63.19	32.86
I_N (A rms)	1.8	23.65	2.06	29.09
Load (Phase A)	4987.4	4916	6973	6845
Load (Phase B)	5001.9	4964	7029	6951
Load (Phase C) (W)	5019.0	2395	7192	3871
Total Load Calculated	15 008	12 275	21 194	17 667

Note: Power Factor = 1.0

TABLE 2. RATED OUTPUT VOLTAGE TESTS

Phase B	0.0 kW	1.5 kW	3.0 kW	4.5 kW	5.0 kW
Balanced 3 Phase Load (kW)	No Load	4.5	9.0	13.5	15.0
V+ to Com V- to Com (Vdc)	142 -142	142 -142	142 -142	142 -142	142 -142
I_{IN} (+)	+1.5	+16.9	31.8	+46.6	51.4
I_{IN} (-) (Adc)	-1.2	-16.5	-31.7	-46.4	-51.3
V_{A-N}	119.3	117.00	116.00	115.1	114.80
V_{B-N}	119.3	116.90	116.00	115.1	114.80
V_{C-N} (V trms)	119.4	117.10	116.20	115.40	115.1
I_A	0	12.07	23.90	35.48	39.28
I_B	0	12.11	24.00	35.73	39.58
I_C	0	12.28	24.26	36.14	40.04
I_N (A rms)	0	0.50	0.945	1.33	1.46
Total Power Calculated (kW)	0	4.26	8.4	12.4	13.7
THD (%)	3.2	2.71	2.4	2.18	2.14

Note: Power Factor = 1.0

TABLE 3. POWER FACTOR AND WAVEFORM TESTS (INDUCTIVE LOADS)

Resistive (kW) per Phase	2.5	3.0	3.5	4.0	4.5	5.0
Inductive (kVAR) per Phase	4.33	4.0	3.57	3.00	2.18	0
Balanced (kVA) 3 Phase Load	15	15	15	15	15	15
Power Factor	0.5	0.6	0.7	0.8	0.9	1.0
V+ to Common	147	147.3	147.4	148.1	148.3	148
V- to Common	147	147.3	147.7	148.1	148.3	148
I_{IN} (+) (Adc)	32.2	35.8	40	44.4	48.8	53.4
I_{IN} (-) (Adc)	33.7	39.2	43.8	47.9	51.8	54.8
I_A (A rms)	41.8	42.1	42.1	42.0	41.7	40.9
I_B (A rms)	42.5	42.9	42.7	42.6	42.1	41.2
I_C (A rms)	43.0	43.3	43.3	43.2	42.8	41.9
I_N (A rms)	0.85	1.16	1.25	1.33	1.30	1.45

TABLE 3. (Concluded)

V_{A-N} (V trms)	119.8	119.9	120	120	119.9	120.1
V_{B-N} (V trms)	120.0	120.0	120.1	120.1	119.9	120.1
V_{C-N} (V trms)	120.1	120.2	120.4	120.3	120.2	120.4
THD (%)	3.6	3.6	3.5	3.35	3.2	2.52

TABLE 4. POWER FACTOR AND WAVEFORM TESTS (CAPACITIVE LOADS)

Resistive (kW) per Phase Setting	0.58	0.75	0.98	1.33	2.06	5.0
Capacitive Load (kVAR) per Phase Setting	1.0	1.0	1.0	1.0	1.0	0
Balanced 3 Phase Load Setting (kVA)	3.46	3.75	4.2	5.0	6.88	15
Power Factor	0.5	0.6	0.7	0.8	0.9	1.0
V_{L-N} (V trms)	120	120	120	120	120	120
V+ to Common (Vdc)	142	142.4	142.6	143.1	144.5	148
V- to Common (Vdc)	142	142.3	142.7	143.1	144.5	148
I_{IN} (+) (Adc)	7.8	9.3	11.4	15.1	23.2	53
I_{IN} (-) (Adc)	8.6	10.2	12.7	16.5	24.1	53.7

TABLE 4. (Concluded)

V_{A-N} (V trms)	120	120	120	120	120	120
V_{B-N} (V trms)	119.9	120	120	119.9	120	120
V_{C-N} (V trms)	120	120	120.1	120	120.1	120.3
I_A (A rms)	9.95	10.56	11.64	13.8	19.16	41.06
I_B (A rms)	10.06	10.66	11.68	13.86	19.33	41.4
I_C (A rms)	10.2	10.8	11.82	14.03	19.54	41.96
I_N (A rms)	0.73	0.73	1.08	1.26	0.94	1.44
THD (%)	3.2	3.23	3.2	3.1	2.71	2.39

TABLE 5. LOW INPUT VOLTAGE TESTS

Input Voltage	±115 Vdc		±90 Vdc	
Power Factor	1.0	0.6	1.0	0.6
Balanced 3 Phase Load (kVA)	15	15	15	15
V+ to Com (Vdc)	115.0	115.0	90.0	90.0
V- to Com (Vdc)	115.0	115.0	90.0	90.0
V_{AN} (V trms)	92.6	93.2	71.8	72.7
V_{BN} (V trms)	92.6	93.4	71.8	72.8
V_{CN} (V trms)	92.8	93.5	71.9	72.9
I_+ (Adc)	41.1	27.9	31.8	21.8
I_- (Adc)	42.1	30.8	32.4	24.5
I_A (A rms)	31.5	32.8	24.3	25.6
I_B (A rms)	31.7	33.4	24.5	26.1
I_C/I_N (A rms)	32.2/1.13	33.8/0.85	24.9/0.92	26.4/0.62
THD (%)	2.5	3.7	2.65	3.9

TABLE 6. RECTIFIER LOAD TESTS

	Half Wave			Full Wave		
		With Transf.				
	No. Transf.	Sl Open	Sl Closed	R	RC	RLC
V+ (Vdc)	142	142	144.6	142	142.4	142.1
V- (Vdc)	142	142	144.5	142	142.2	142.1
I+ (Adc)	17.8	20.9	18.7	15.6	15.4	15.7
I- (Adc)	4.3	3.5	3.7	15	15.9	14.9
I_A (A rms)	13.2	14.8	13.4	11.4	12.85	11.4
I_B (A rms)	13.2	14.8	13.7	11.4	13.01	11.4
I_C (A rms)	13.5	14.8	13.6	11.6	13.34	11.6
I_N (A rms)	17.3		17.5			
I_{out} (Adc)	16.3	15.5	15.9	14.2	15.4	13.8
V_{out} (Vdc)	152.5	150.1	152.5	271.2	273	271
Output (V_{pp}) Ripple	3.5	3	3.5	40	0.6	0.5[a]
V_{A-N} (V trms)	118.1	117.9	120.1	117.7	118.6	117.7

TABLE 6. (Concluded)

	Half Wave			Full Wave		
		With Transf.				
	No. Transf.	S1 Open	S1 Closed	R	RC	RLC
V_{B-N} (V trms)	118.1	117.9	120	117.6	118.6	117.6
V_{C-N} (V trms)	118.1	118	120.2	117.8	118.7	117.8
THD (%)	4.95	5	4.98	3.65	4.8	3.88
Load Setting (kW)	2	2	2	4	4	4
Load Calculated (kW)	2.49	2.33	3.42	3.85	4.2	3.74

a. Ripple measured before L and C was 38 V_{pp}.

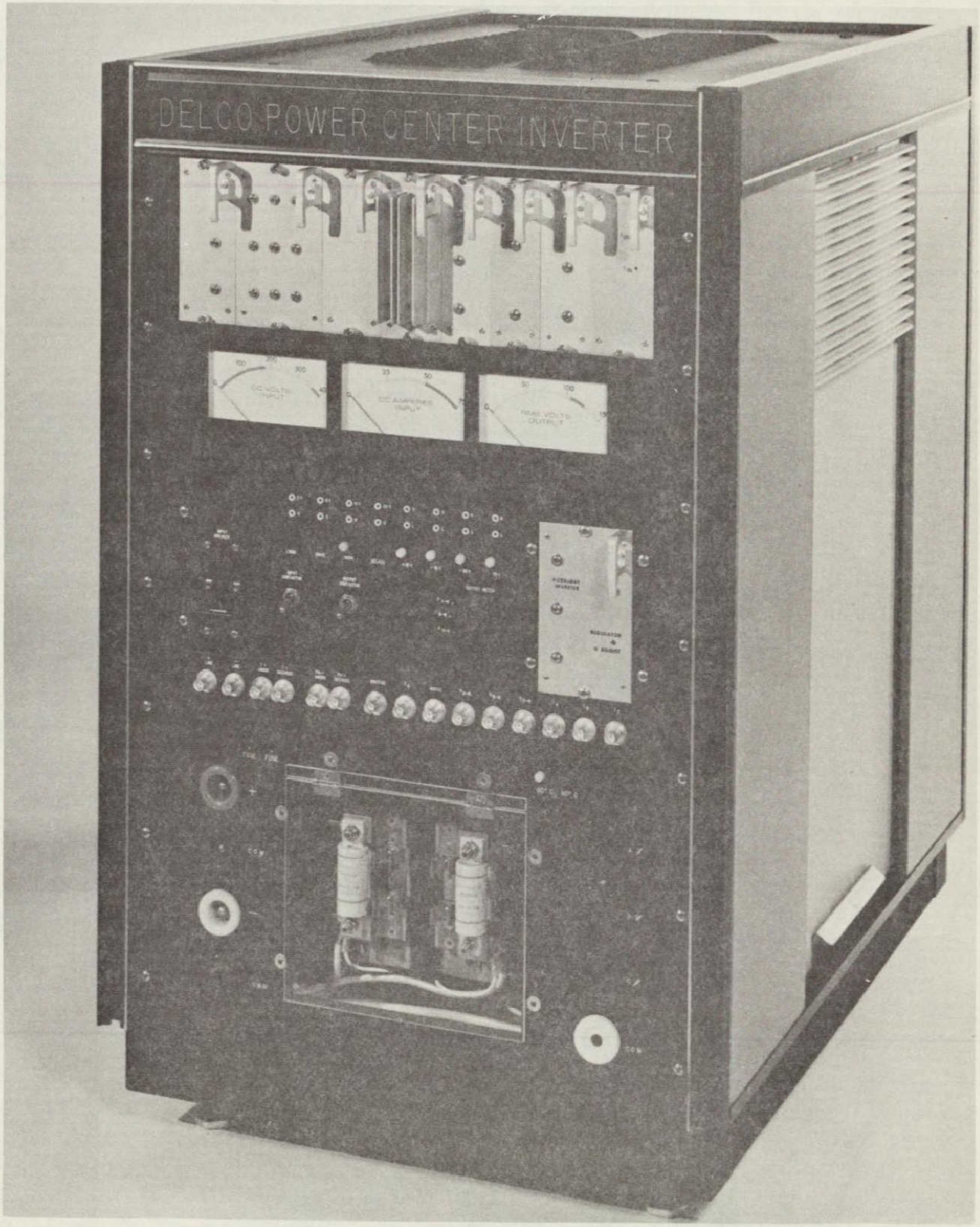


Figure 1. ADM-006 inverter.

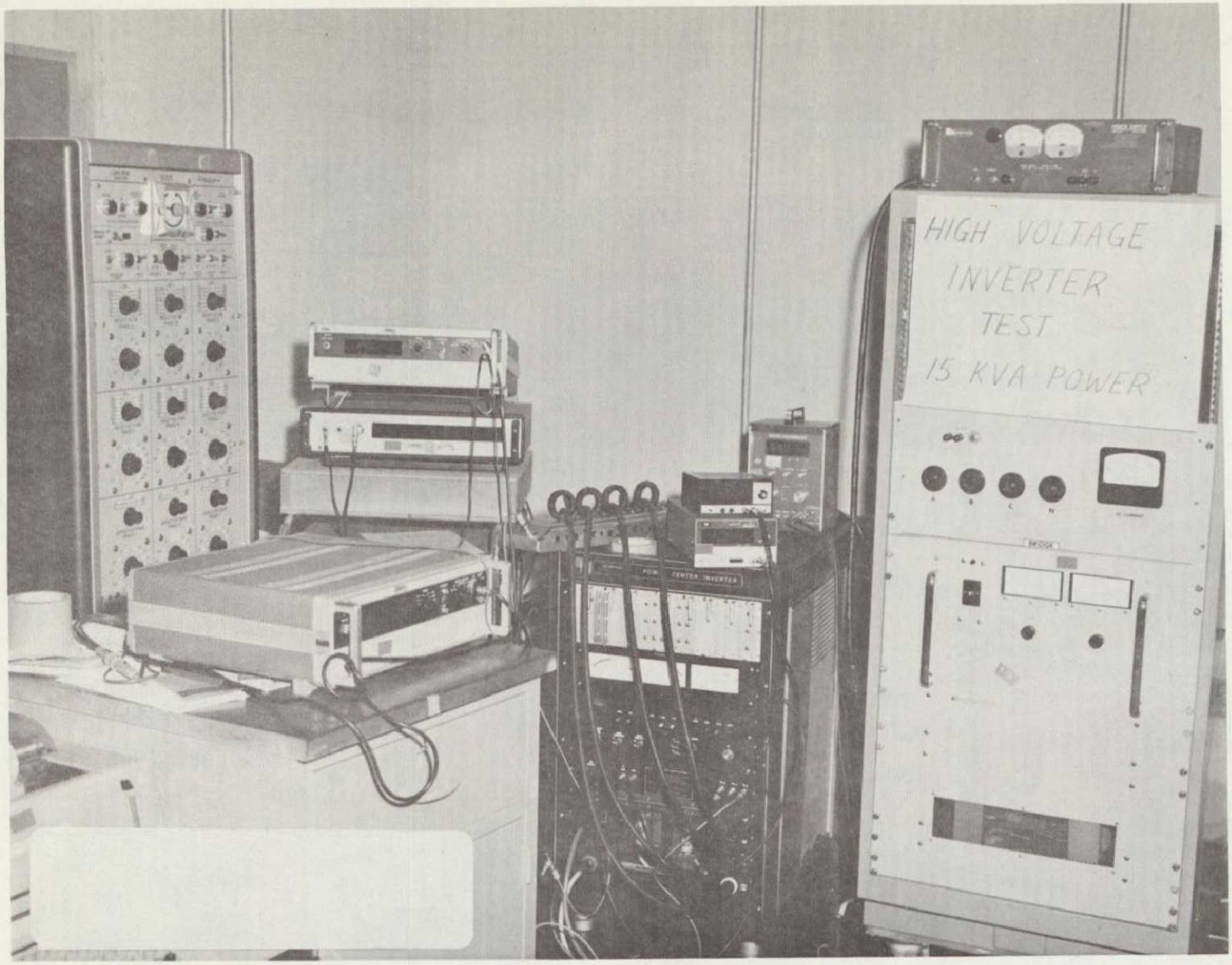


Figure 2. Laboratory test setup for ADM-006.

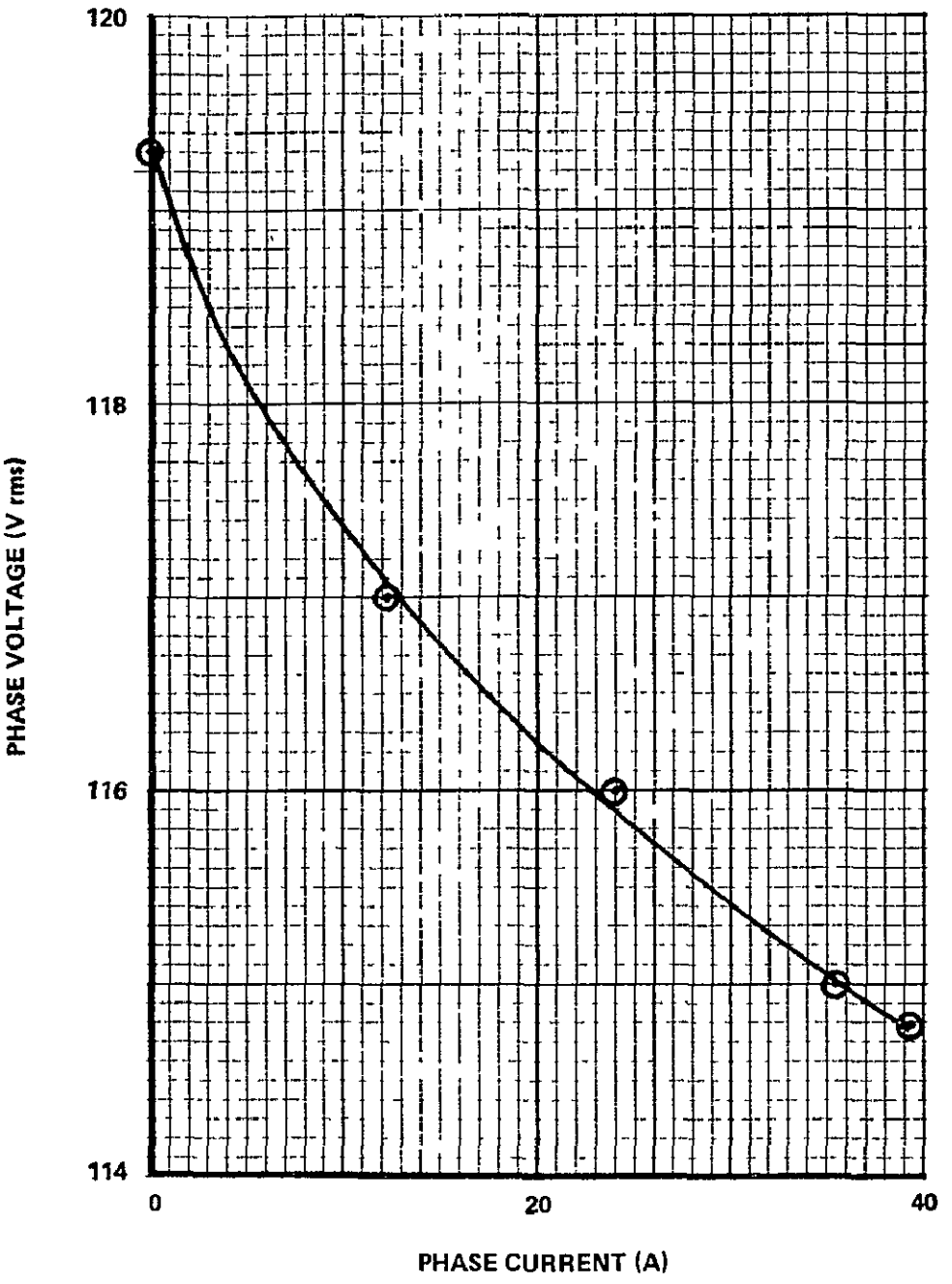


Figure 4. Output voltage for Phase A as a function of current for unity power factor load.

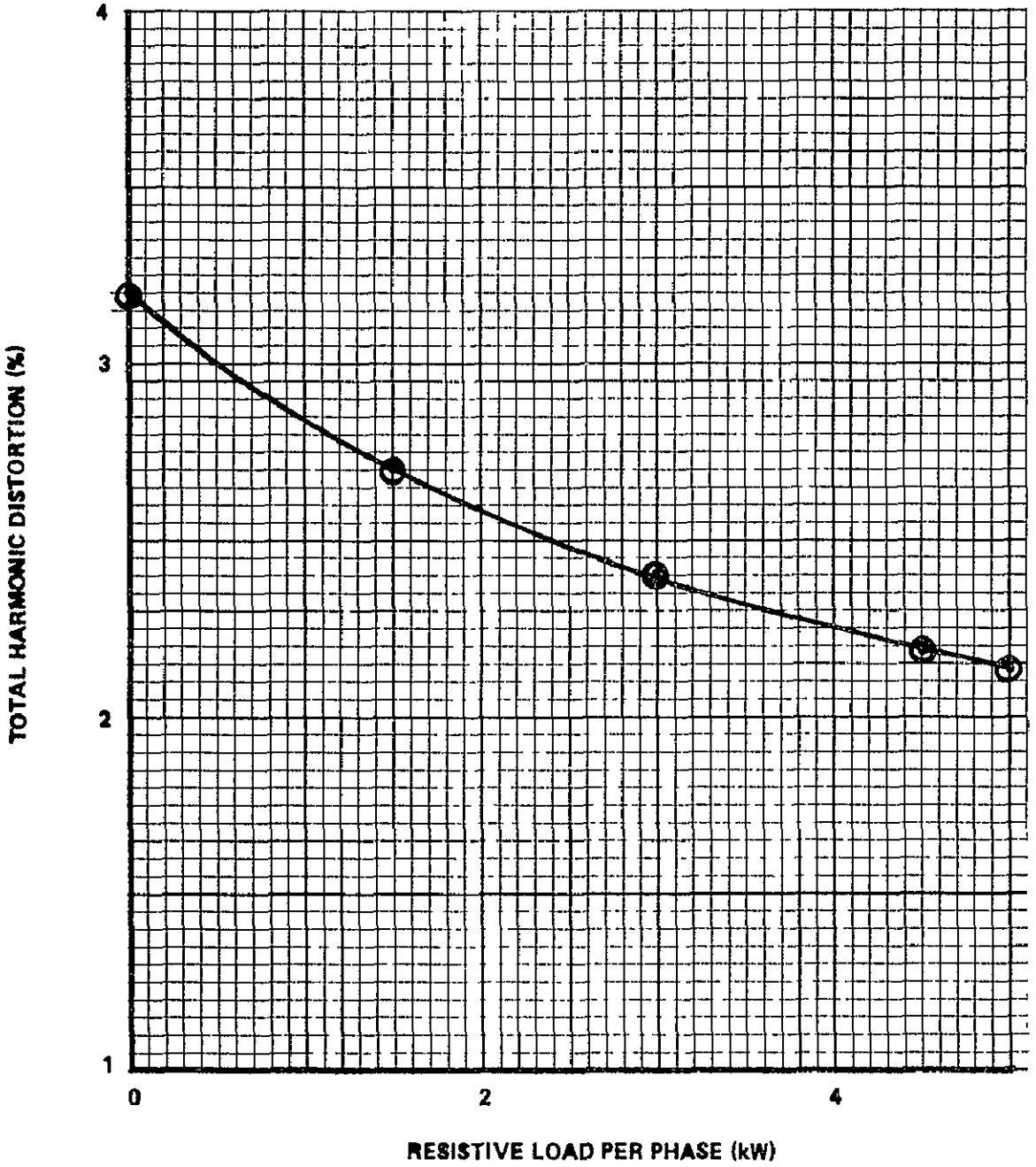


Figure 5. Waveform distortion as a function of resistive loading.

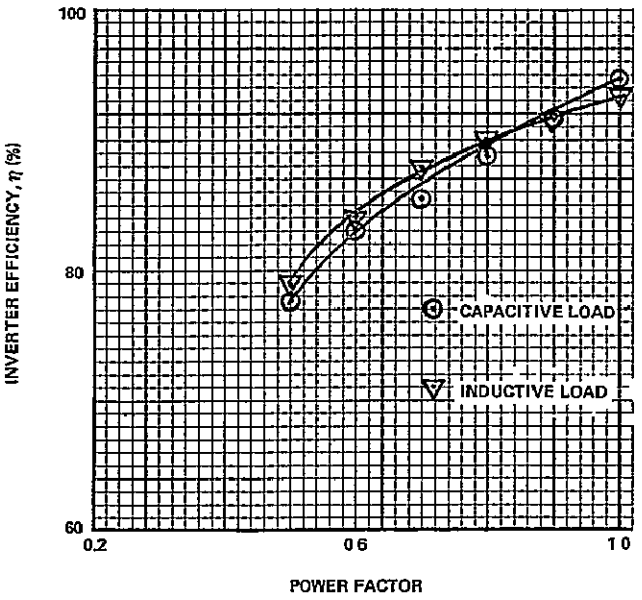


Figure 6. Inverter efficiency as a function of power factor.

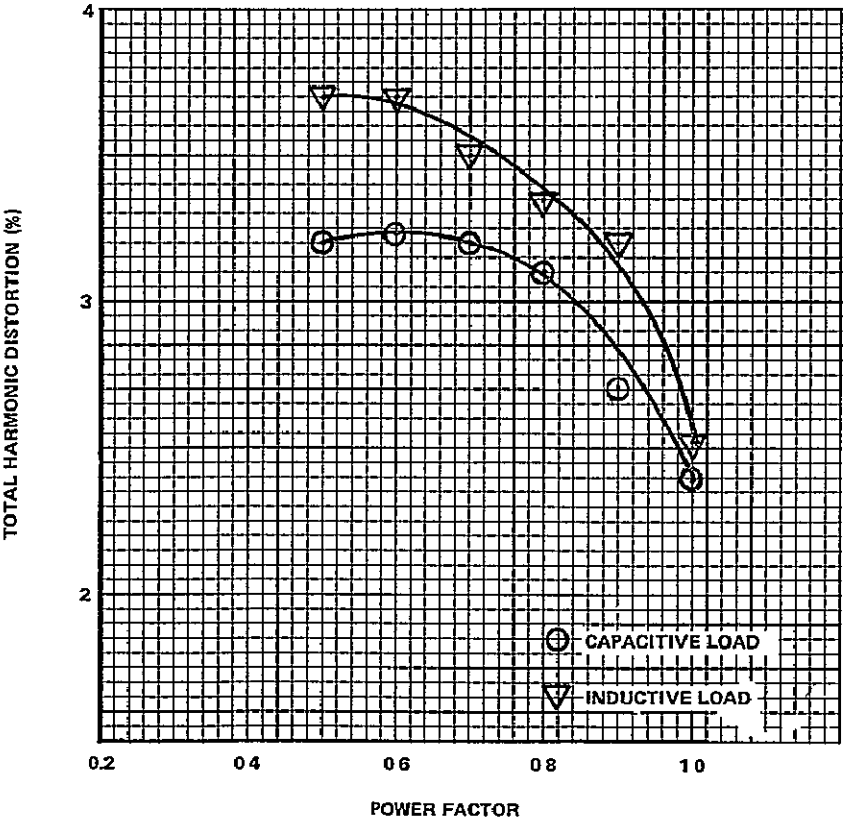


Figure 7. Total harmonic distortion as a function of power factor.

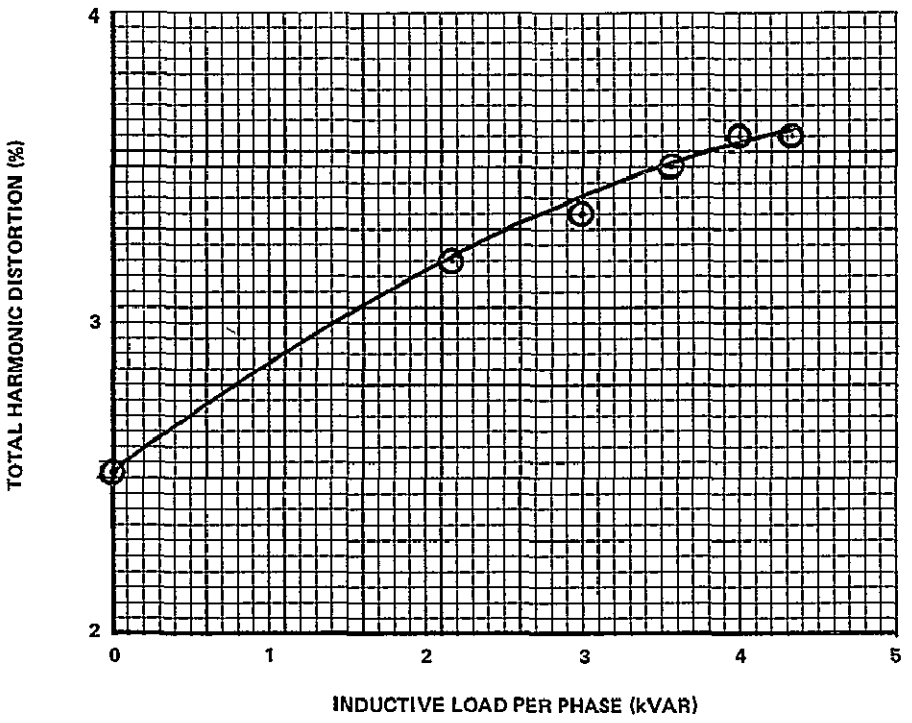


Figure 8. Total harmonic distortion as a function of inductive loading.

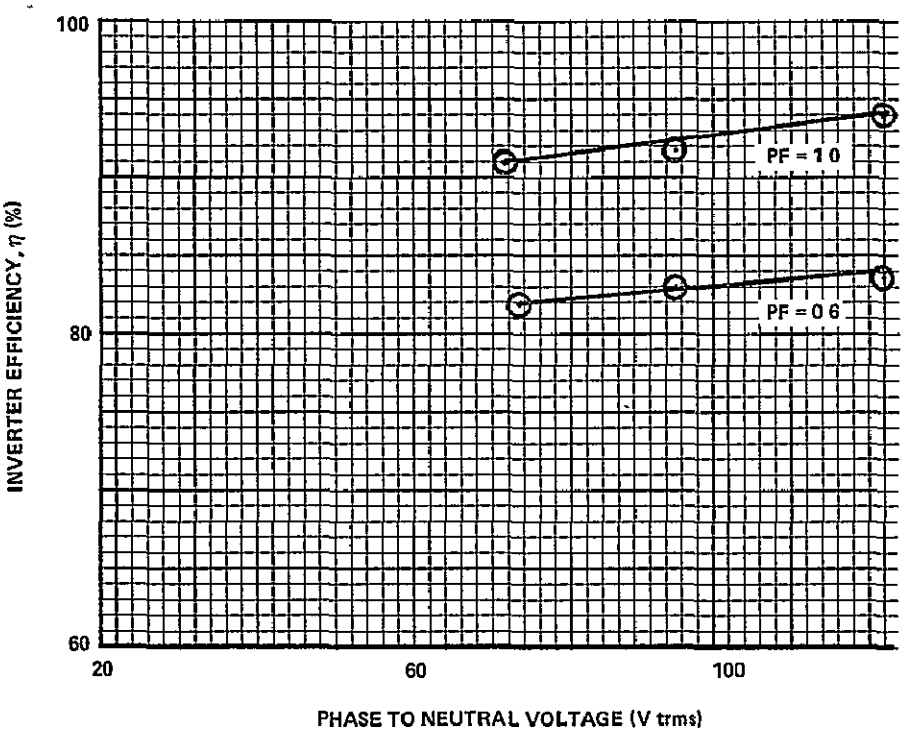
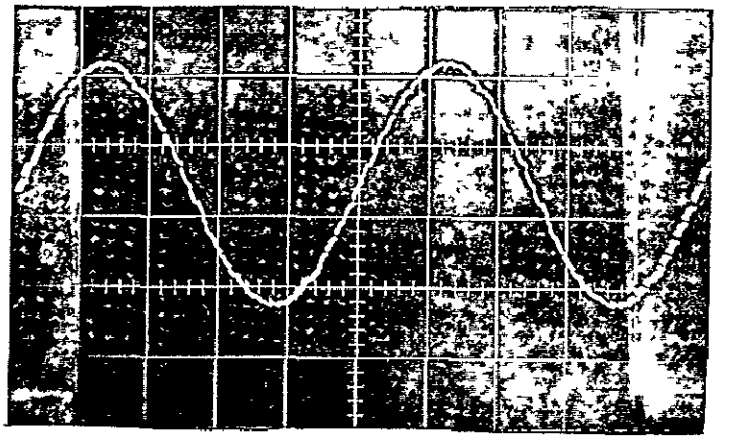
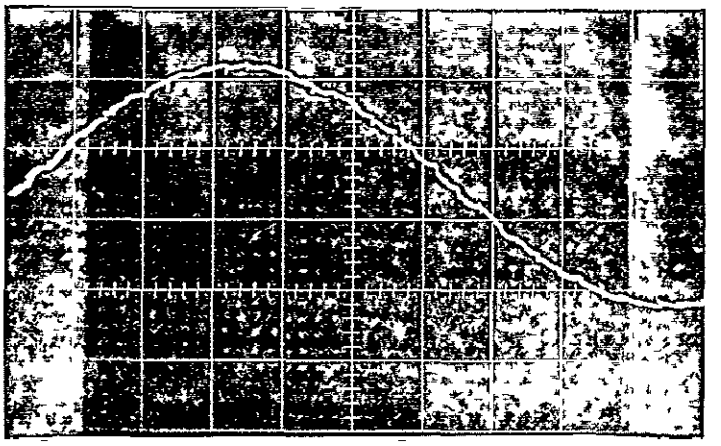


Figure 9. Inverter efficiency as a function of output voltage for constant load impedance.



100 V/cm

0 5 ms/cm



0 2 ms/cm

Figure 10. Phase A output voltage for 15 kW resistive load.

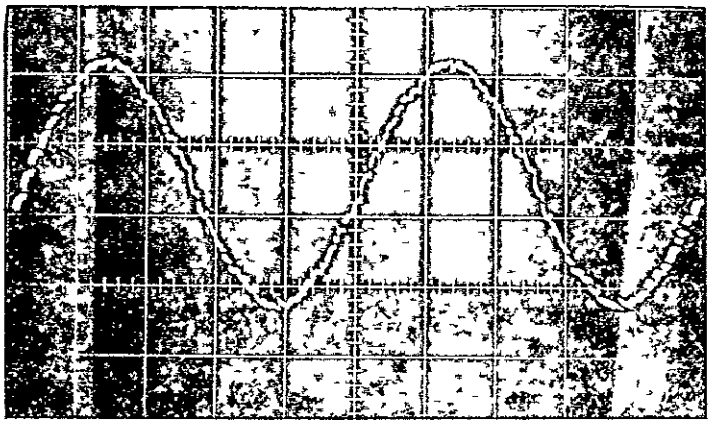
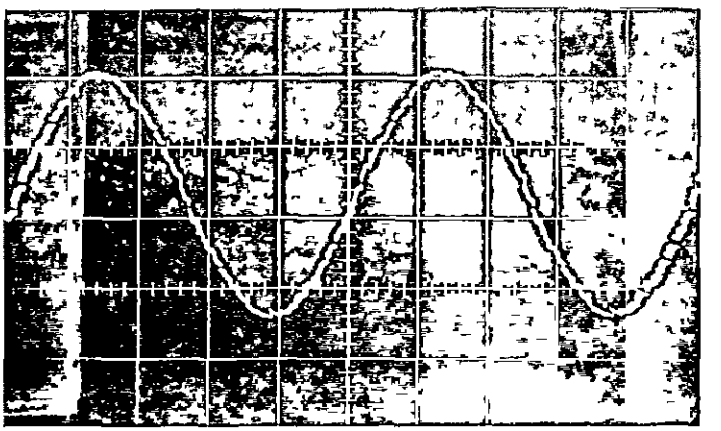
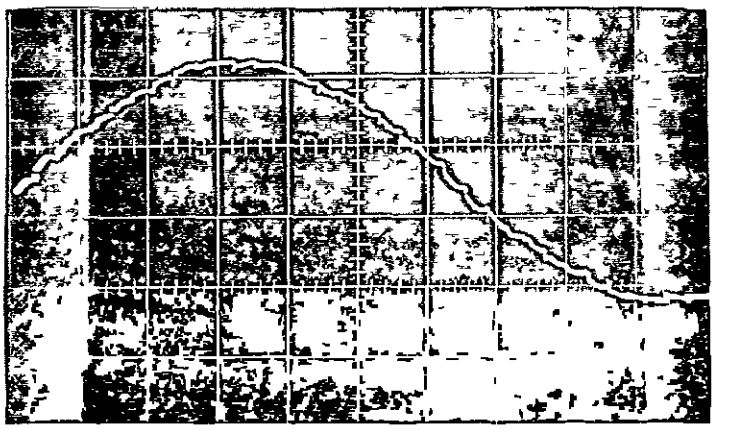


Figure 11. Phase A output voltage for 15 kVA inductive load at 0.5 power factor.



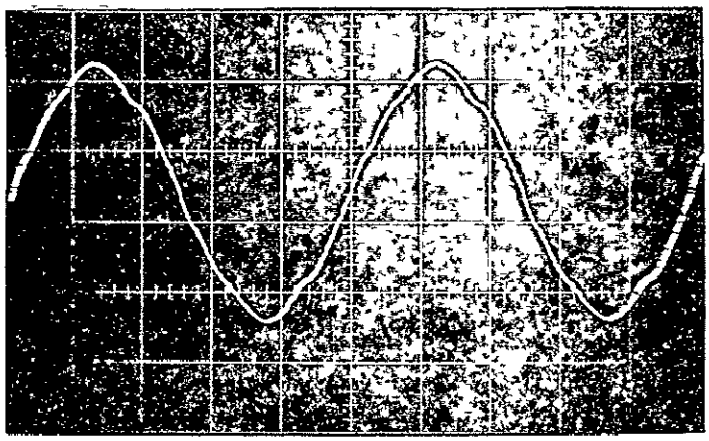
0 5 ms/cm

100 V/cm



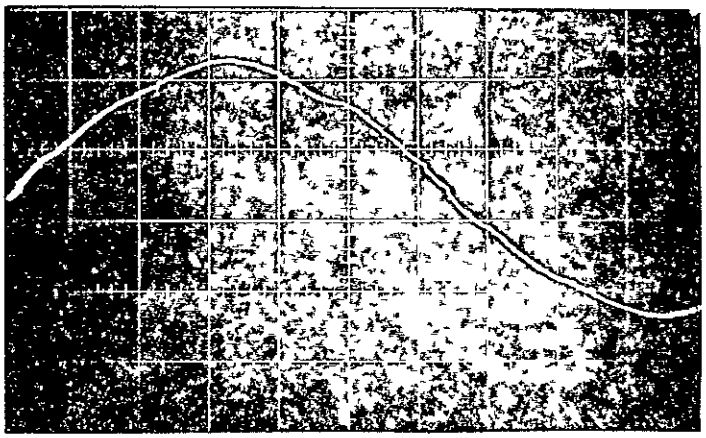
0 2 ms/cm

Figure 12. Phase A output voltage for 15 kVA inductive load at 0.9 power factor.



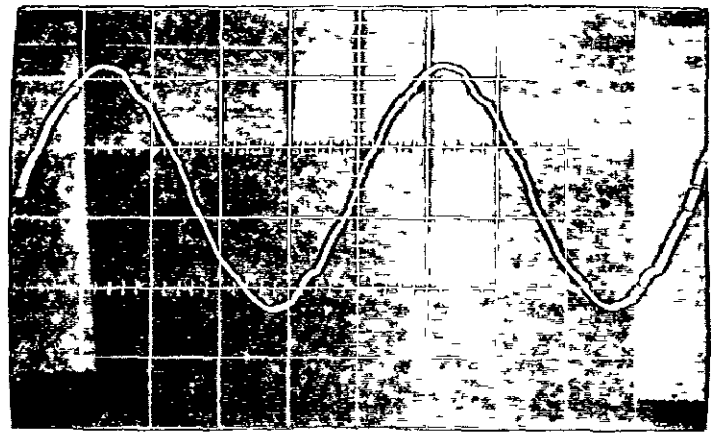
0 5 ms/cm

100 V/cm



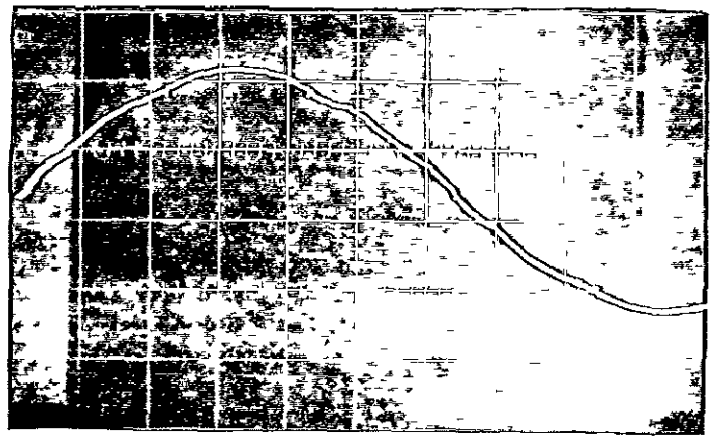
0 2 ms/cm

Figure 13. Phase A output voltage for 15 kVA capacitive load at 0.5 power factor.



0 5 ms/cm

100 V/cm



0 2 ms/cm

Figure 14. Phase A output voltage for 15 kVA capacitive load at 0.9 power factor.

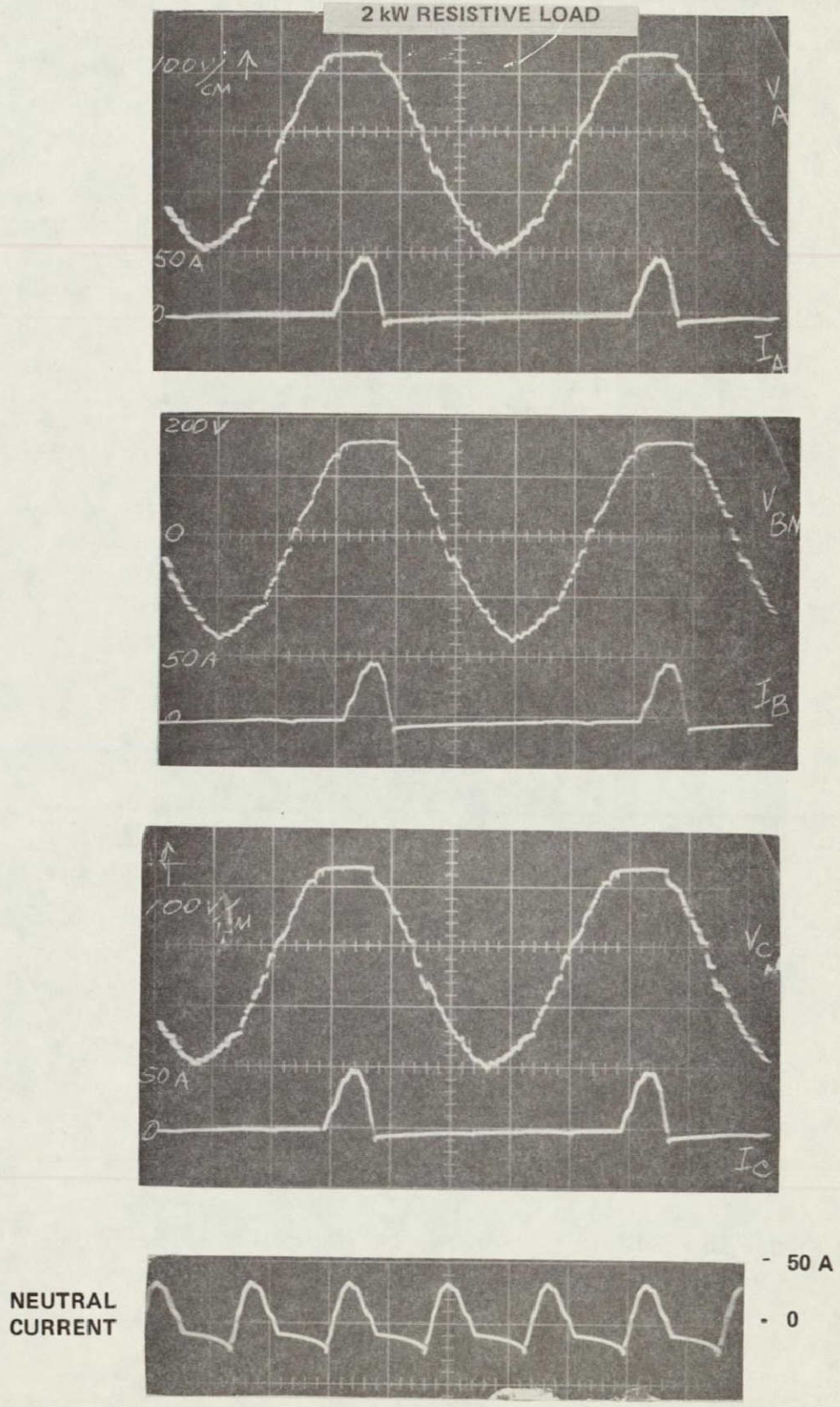
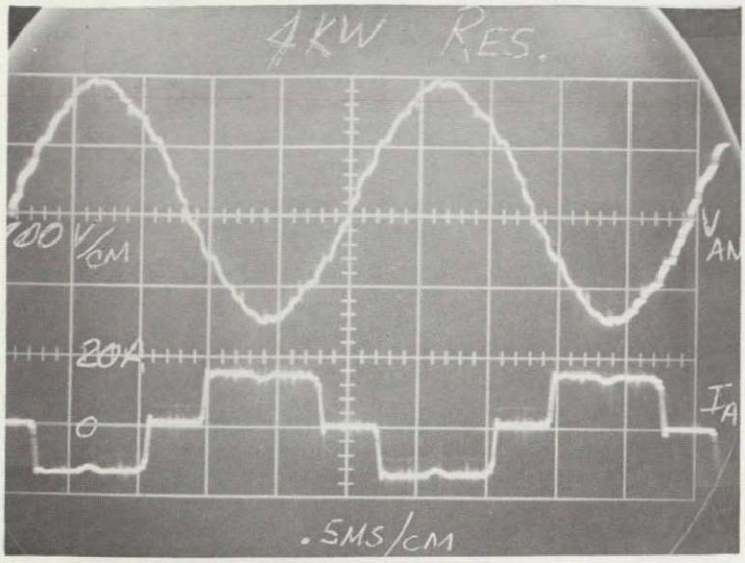
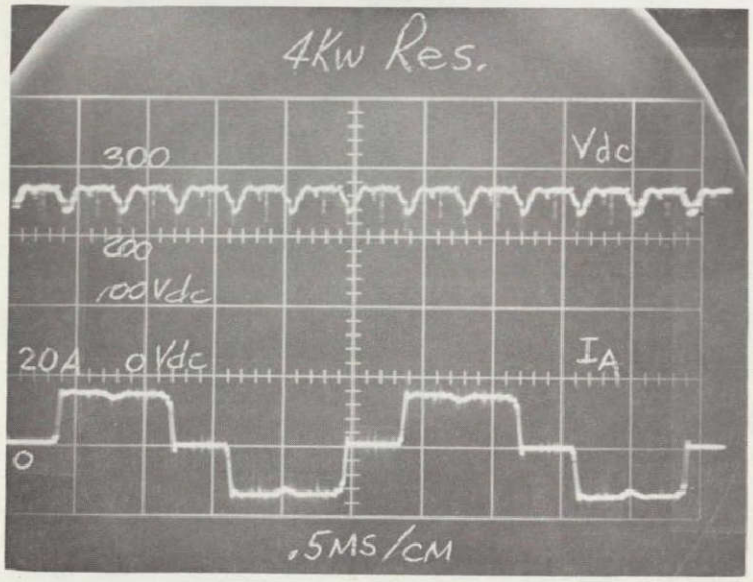


Figure 15. Output voltages and phase currents of inverter into pure resistive load half wave rectified.

4 kW PURE RESISTIVE

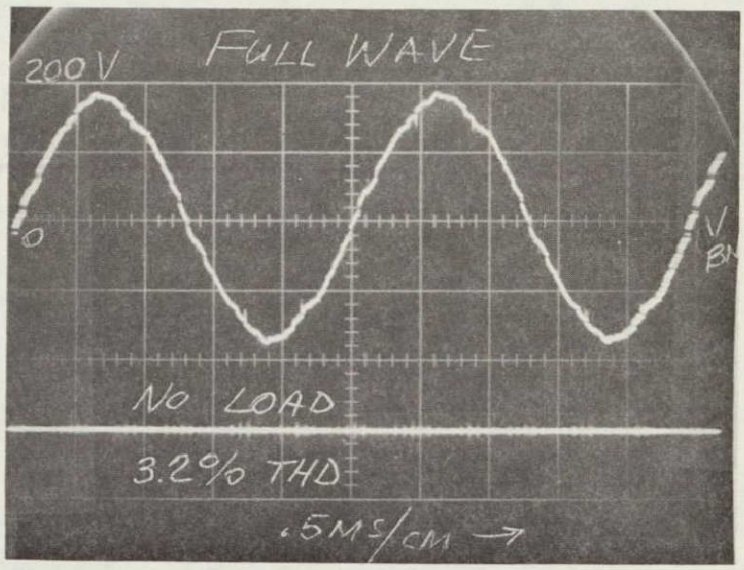




40 $V_{pk\text{-}pk}$ RIPPLE

Figure 16. Full wave rectified operation without filtering.

4 kW RESISTIVE LOAD



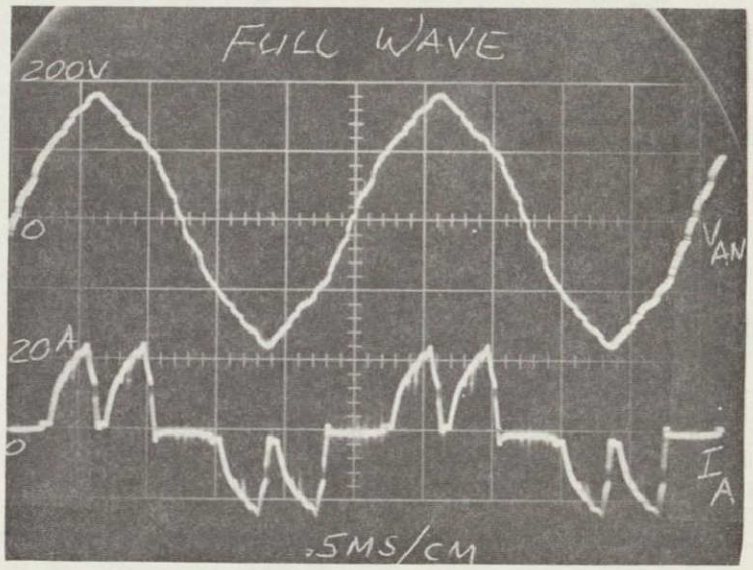


Figure 17. Full wave rectified operation with filtering.

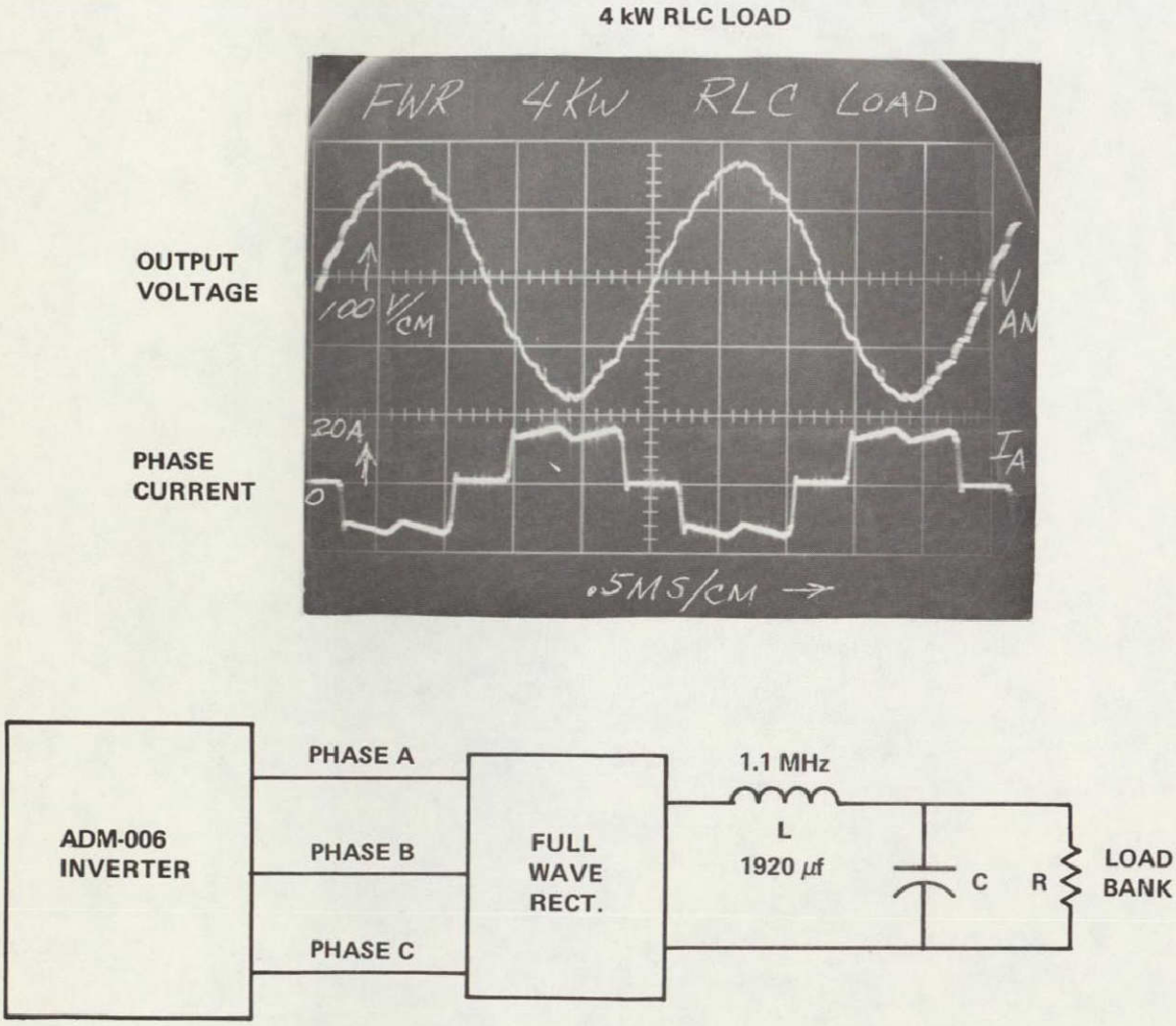


Figure 18. Full wave rectified operation with RLC load.

DELCO ELECTRONICS
MODEL ADM-006 INVERTER
SPECIFICATION

Characteristics and Performance

Required Input. ±142 V dc (high power source)
120 V ac, 60 Hz (less than 300 mW for low power control electronics)

Output (120/208 400 Hz):	Balanced Load	Maximum Load per Phase	Maximum Load Unbalance per Phase
Continuous	15 KVA	5.0 KVA	3 KVA
Intermittent	25 KVA	8.3 KVA	4 KVA

Load Power Factor: Unity to Zero, leading or lagging

Voltage Regulation: (open loop) 3.3%

Distortion: 4% THD

Ambient Air Temperature: $10^{o}C$ to $50^{o}C$ forced air cooled

Size. 19"W, 28"H, 29-1/2" D (Enclosed rack cabinet)

Weight:	
Cabinet	100 lbs.
Inverter & Breadboard Structure	125 lbs.
Total	225 lbs.

Efficiency: 94%

APPENDIX B

TEST PROCEDURE 40M22460

MSFC FORM 422 (VERTICAL) (AUGUST 1990)

NOTICE—When Government drawings, specifications or other data are used for any purpose other than in connection with a definitely related Government procurement operation the United States Government thereby incurs no responsibility nor obligation whatsoever and the fact that the Government may have formulated furnished or in any way supplied the said drawings specifications or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation or conveying any rights or permission to manufacture use or sell any patented invention that may in any way be related thereto

APPLICATION		PART No	MF
NEXT ASSY	USED ON		

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TEST PROCEDURE

POWER CENTER INVERTER

(ADM-006)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: FRACTIONS DECIMALS ANGLES	ORIGINAL DATE OF DRAWING 2/15/75 DRAFTSMAN / CHECKER TRACER / CHECKER ENGINEER G V. / ENGINEER	TEST PROCEDURE POWER CENTER INVERTER (ADM-006)	GEORGE C MARSHALL SPACE FLIGHT CENTER NATIONAL AERONAUTICS AND SPACE ADMINISTRATION HUNTSVILLE ALABAMA
MATERIAL	SUBMITTED Buddy V. Simpson		
HEAT TREATMENT			
FINAL PROTECTIVE FINISH	APPROVED W. Farmer Jr.	SCALE / UNIT WT	DWG SIZE A / 40M22460 / SHEET 1 OF 22

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1. PURPOSE

1.1 The purpose of this test procedure is to specify the test methods for the verification testing of the Power Center Inverter (ADM-006) built by Delco Electronics Division, General Motors Corporation under Contract NAS8-28645

2. SCOPE

2.1 This procedure specifies the methods for testing the ADM-006 under simulated loading conditions similar to those which might be expected during normal use. Methods for performing the following tests are specified herein

(a) rated power output tests

(b) rated output voltage tests

(c) power factor and waveform tests

(d) low input voltage tests

(e) rectifier load tests.

3. REFERENCES

3.1 The following documents form a part of this test procedure to the extent specified herein Unless otherwise indicated, the issue in effect on the date of invitation for bids or request for proposals shall apply.

STANDARDS

MIL-STD-831 Test Reports, Preparation of

DRAWINGS

George C Marshall Space Flight Center

TBD

(Copies of specifications, standards, drawings, and publications required by contractors in connection with the application of this procedure should be obtained from the procuring activity or as directed by the contracting officer.)

4. ABBREVIATIONS

Not applicable

5. RESPONSIBILITIES

5.1 Electronics and Control Laboratory - The Power Branch (EC12) or their representative shall be responsible for the implementation of this procedure.

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6. PROCEDURES

6 1 Test Setup

6 1.1 Source Voltage Setup

(a) Connect four HP6475A power supplies to ADM-006 as specified in figure 1.

(b) Set all ON-OFF breakers on power supplies to OFF

6.1.2 ADM-006 Setup

(a) Set INPUT BREAKER to OFF

(b) Set AUXILIARY 60 Hz switch to OFF

(c) Set INPUT CONTACTOR switch to OFF

(d) Set OUTPUT CONTACTOR switch to OFF

(e) Connect ADM-006 to 120 VAC/60 Hz power

6.1.3 Avtron Model T938 Load Bank Setup for 400 Hz Operation

(a) Set all KW and KVAR dials to indicate zero.

(b) Set COOLING AIR BLOWER switch to START The "Cooling Air Blower" lamp, "Cooling Air Failure" Lamp, the cooling alarm, and the "Air Failure Time Delay" will come on momentarily When sufficient cooling air is being supplied by the fan, the three air failure indicators will turn off and the "Cooling Air Blower" lamp will remain lit.

(c) Set the AIR FAILURE TIME DELAY to desired delay This can be set between zero and five minutes.

(d) Set the MASTER LOAD switch to OFF

(e) Set the individual phase switches, PHASE A, PHASE B, and PHASE C, to ON

(f) Set MODE switch to BALANCED 3 PHASE. In this position real loading and reactive loading is applied to all three phases by adjusting the control switches for KW and KVAR respectively under PHASE B to the desired value.

(g) Set the COOLING SYSTEM PROTECTION switch to ON.

(h) Set the LOW FREQUENCY PROTECTION switch to ON.

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6.1.3 Avtron Model T938 Load Bank Setup (Cont'd)

(i) Set the FREQUENCY switch to 400 Hz.

(j) Set heater switch to ON.

(k) Set the Vernier INHIBIT Switch to OFF.

6.1.4 Test Connections

(a) Connect inverter to load bank as specified in figure 1.

(b) Connect a DVM (Fairchild 7050 or equivalent) between V+ and common as specified in figure 1.

(c) Connect a DVM (Fairchild 7050 or equivalent) between V- and common as specified in figure 1.

(d) Connect a distortion analyzer (Hewlett Packard Model 302A or equivalent), as specified in figure 1.

(e) Connect a voltmeter (Fluke 9500A or equivalent) from PHASES A, B, and C to Neutral as indicated in figure 1.

6.1.5 Test Equipment

6.1.5.1 Instruments

Digital Voltmeter, Fairchild 7050, 2 Ea.

Voltmeter, true RMS, Fluke 9500A

Distortion Analyzer, HP331A

6.1.5.2 Components

Diode, IN 1189, 6 Ea.

Capacitor, 480 u f, 125 V, 36 Ea.

Resistor 604K, 3 Ea.

Auto transformer, variable, 3 phase, 400 Hz, General Radio Co., Model M20G3

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6 2 Rated Power Output Tests

(a) Set the Resistive KW Phase B control switch on the load bank to 5 0 KW This automatically sets phases A and C to 5 0 KW

(b) Set the AUXILIARY 60 Hz switch on the ADM-006 to ON

(c) Set the ON-OFF breakers on the HP6475A power supplies to ON

(d) Adjust supplies for V+ of +142Vdc and V- of -142 Vdc as indicated on the two test meters

(e) Set the INPUT BREAKER on the ADM-006 to ON

(f) Set the INPUT CONTACTOR on the ADM-006 to ON

(g) Set OUTPUT CONTACTOR to ON

(h) Set the MASTER LOAD switch on the load bank to ON

(i) Monitor operation for a minimum of two hours as test for continuous rating

(j) Fill in values in Column II of Table I

(k) At completion of continuous balanced rating test, set MASTER LOAD switch on the load bank to OFF and the OUTPUT CONTACTOR on the ADM-006 to OFF

(l) Set MODE switch on the load bank to IND PHASE In this position loading of each phase is controlled by adjusting the individual control switches

(m) Set Resistive KW PHASE A and PHASE B to 5 0 KW and PHASE C to 2 0 KW

(n) Repeat steps (g) through (i)

(o) Fill in values in Column III of Table I

(p) At the completion of continuous unbalanced rating test, set the MASTER LOAD switch on the load bank to OFF and the OUTPUT CONTACTOR on the ADM-006 to OFF

(q) Set MODE switch on load bank to BAL 3 PHASE and set RESISTIVE KW PHASE B to 8 0 KW This automatically sets Phases A and C to 8 0 KW

(r) Set OUTPUT CONTACTOR on ADM-006 to ON and MASTER LOAD switch on load bank to ON

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6 2 Rated Power Output Tests (Cont'd)

(s) Monitor operation for one minute as test for intermittent rating Fill in the values in column IV of Table I

(t) At the completion of the balanced intermittent test set the MASTER LOAD switch on the load bank to OFF and the OUTPUT CONTACTOR on ADM-006 to OFF Failure to disconnect the load after intermittent test may result in damage to the inverter

(u) Set MODE switch on load bank to IND PHASE, and set RESISTIVE KW PHASE A and PHASE B to 8 0 KW and PHASE C to 4 0 KW

(v) Set OUTPUT CONTACTOR on ADM-006 to ON and MASTER LOAD switch on load bank to ON

(w) Monitor operation for one minute as test for intermittent rating Fill in the values in Column V of Table I

(x) Set MASTER LOAD switch on load bank to OFF and OUTPUT CONTACTOR on ADM-006 to OFF Failure to disconnect the load after intermittent test may result in damage to the inverter

6.3 Rated Output Voltage Tests

(a) Set MODE switch on load bank to BAL 3 PHASE

(b) Set RESISTIVE KW PHASE B to zero KW. This automatically sets Phases A and C to zero KW

(c) Set OUTPUT CONTACTOR on ADM-006 to ON

(d) Set MASTER LOAD switch on load bank to ON

(e) Measure and record the values indicated in Table II

(f) Set MASTER LOAD switch on load bank to OFF

(g) Set OUTPUT CONTACTOR on ADM-006 to OFF

(h) Repeat steps (c) through (g) with RESISTIVE KW PHASE B set to each of the values specified in Table II Phases A and C are set automatically to the value of Phase B

(i) Determine voltage regulation Voltage regulation no load to full load shall be less than 4 5 percent

6 4 Power Factor and Waveform Tests

6.4 1 Inductive Loading

(a) Set MODE switch on load bank to BAL 3 PHASE

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6 4 1 Inductive Loading (Cont'd)

(b) Set the REACTIVE LOAD switch to INDUCTIVE.

(c) Set RESISTIVE KW PHASE B to 4.62 KW This automatically sets Phases A and C to 4 62 KW

(d) Set INDUCTIVE KVAR PHASE B to 8 0 KVAR This automatically sets Phases A and C to 8 0 KVAR

(e) Set OUTPUT CONTACTOR on ADM-006 to ON

(f) Set MASTER LOAD switch on load bank to ON

(g) Measure and record the values indicated in Table III for a power factor of 0 5 Total harmonic distortion shall not be greater than 4 0 percent

(h) Set MASTER LOAD switch on load bank to OFF

(i) Set OUTPUT CONTACTOR on ADM-006 to OFF

(j) Repeat steps (d) through (i) with RESISTIVE KW PHASE B and INDUCTIVE KVAR PHASE B adjusted to each of the values indicated in Table III Phases A and C will be set automatically to the same value as Phase B as long as the Mode switch is in the BAL 3 PHASE position

6.4 2 Capacitive Loading

(a) Set REACTIVE LOAD switch on load bank to CAPACITIVE

(b) Set MODE switch to BAL 3 PHASE.

(c) Set RESISTIVE KW PHASE B to 0.58 KW This automatically sets Phases A and C to 0 58 KW

(d) Set CAPACITIVE KVAR PHASE B to 1.0 KVAR This automatically sets Phases A and C to 1 0 KVAR

(e) Set OUTPUT CONTACTOR on ADM-006 to ON

(f) Set MASTER LOAD switch on load bank to ON

(g) Measure and record the values indicated in Table IV for a power factor of 0 5 Total harmonic distortion shall not exceed 4 0 percent.

(h) Set MASTER LOAD switch on load bank to OFF

(i) Set OUTPUT CONTACTOR on ADM-006 to OFF

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6 4 2 Capacitive Loading (Cont'd)

(j) Repeat steps (e) through (j) with RESISTIVE KW PHASE B and CAPACITIVE KVAR PHASE B adjusted to each of the values indicated in Table IV Phases A and C will be set automatically to the same value as Phase B as long as the MODE switch is in the BAL 3 PHASE position

6 5 Low Input Voltage Tests

(a) Adjust the output controls of the HP6475A power supplies to obtain a balanced input of ± 115 Vdc to the ADM-006

(b) Set the mode switch on load bank to BAL 3 PHASE

(c) Set all inductive and capacitive KVAR controls to zero

(d) Set RESISTIVE KW PHASE B to 5 0 KW This automatically sets Phases A and C to 5 0 KW.

(e) Set the OUTPUT CONTACTOR on ADM-006 to ON

(f) Set the MASTER LOAD switch on the load bank to ON

(g) Measure and record the values indicated in Table V for the indicated input voltage and a power factor of 1 0

(h) Set MASTER LOAD switch on load bank to OFF

(i) Set the OUTPUT CONTACTOR on ADM-006 to OFF

(j) Set the REACTIVE LOAD switch to INDUCTIVE

(k) Set INDUCTIVE KVAR PHASE B to 6 67 KVAR This automatically sets phases A and C to 6 67 KVAR

(l) Set the OUTPUT CONTACTOR on ADM-006 to ON

(m) Set the MASTER LOAD switch on load bank to ON

(n) Measure and record the values indicated in TABLE V for the indicated input voltage and a power factor of 0 6

(o) Set MASTER LOAD switch on load bank to OFF

(p) Set the OUTPUT CONTACTOR on ADM-006 to OFF

(q) Repeat steps (b) through (p) for an input of ± 90 Vdc to the ADM-006

(r) Readjust power supplies for ± 142 Vdc input to ADM-006

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6.6 Rectified Output Test

6.6.1 Avtron Model T938 Load Bank Setup for DC Operation

CAUTION:

All autotransformers (verniers) located on the Load Bank Control Panel must be disabled before applying DC voltage to the load bank. The VERNIER INHIBIT Switch disables the Resistive Verniers and must be ON during test. The REACTIVE LOAD Switch disables the Inductive and the capacitive Verniers and must be in the OFF position during test. Failure to observe this caution will result in permanent damage to the autotransformers.

(a) Set MASTER LOAD Switch to OFF.

(b) Set VERNIER INHIBIT Switch to ON.

(c) Set REACTIVE LOAD Switch to OFF.

(d) Set all KW and KVAR dials to indicate ZERO.

(e) Set COOLING AIR BLOWER Switch to START.

(f) Set COOLING SYSTEM PROTECTION switch to ON.

(g) Set AIR FAILURE TIME DELAY to three (3) minutes.

(h) Set individual phase switches, PHASE A, PHASE B, and PHACE C to ON.

(i) Set MODE switch to BALANCED 3 PHASE.

CAUTION. Maintain MODE switch in BALANCED 3 PHASE position. With mode switch in individual phase position, unbalanced loading is possible which could result in excessive current in relay contacts in the load bank.

(j) Set LOW FREQUENCY PROTECTION switch to BYPASS.

(k) Set HEATER switch to ON.

6.6.2 Half-Wave Rectifier

(a) Set up test equipment in accordance with figure 2. The filter used shall be as shown in figure 5.

(b) Set the AUXILIARY 60 HZ switch on the ADM-006 to ON.

(c) Set the input voltage to the ADM-006 to $\pm$ 142 Vdc.

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(d) Set the INPUT BREAKER on the ADM-006 to ON.

(e) Set the INPUT CONTACTOR on the ADM-006 to ON.

(f) Set the OUTPUT CONTACTOR on the ADM-006 to ON.

(g) Set the RESISTIVE KW PHASE B selector on the load bank control panel to 2 DC (special marking).

(h) Set the MASTER LOAD switch on the load bank control panel to ON.

(i) Measure and record the values indicated in Table VI in the half-wave column.

(j) Set the MASTER LOAD switch to OFF.

(k) Set the OUTPUT CONTACTOR TO OFF.

6.6.3 Full-Wave Rectifier

(a) Set up test equipment in accordance with figure 3. The filter used shall be as shown in figure 5.

(b) Set the OUTPUT CONTACTOR on the ADM-006 to ON.

(c) Set the RESISTIVE KW PHASE B selector on the load bank control panel to 4 DC (special marking).

(d) Set the MASTER LOAD switch on the load bank control panel to ON.

(e) Measure and record the values indicated in table VI in the full-wave column.

(f) Set the MASTER LOAD switch to OFF.

(g) Set the OUTPUT CONTACTOR to OFF.

6.6.4 Transformer Rectifier Loads

(a) Set up test equipment in accordance with figure 4. The filter used shall be as shown in figure 5.

(b) Set the OUTPUT CONTACTOR on the ADM-006 to ON.

(c) Adjust the Variac to obtain an output voltage of (TBD) Vdc.

(d) Set the RESISTIVE KW PHASE B selector on the load bank control panel to 2 DC (special marking).

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(e) Set the MASTER LOAD switch on the load bank control panel to ON.

(f) Measure and record the values indicated in table VI in the transformer-rectifier column.

(g) Set the MASTER LOAD switch to OFF.

(h) Set the OUTPUT CONTACTOR to OFF.

(i) Remove all power to the system.

7. REPORTS

7.1 At the completion of the verification tests, a test report shall be prepared in accordance with Standard MIL-STD-831. The report shall include all test data and results. A reproducible copy of all data sheets shall be supplied to the procuring activity.

8. MODIFICATIONS OR CHANGES

8.1 Recommendations for modifications or changes to the procedures specified herein shall be submitted in writing to the Chief, Power Branch (EC12), Marshall Space Flight Center, Alabama 35812.

Custodian:

EC12
NASA/George C. Marshall
Space Flight Center

Preparing Activity:

EC12
George C. Marshall
Space Flight Center

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MSFC FORM 422-8 (VERTICAL) (NOVEMBER 1962) CONTINUATION SHEET

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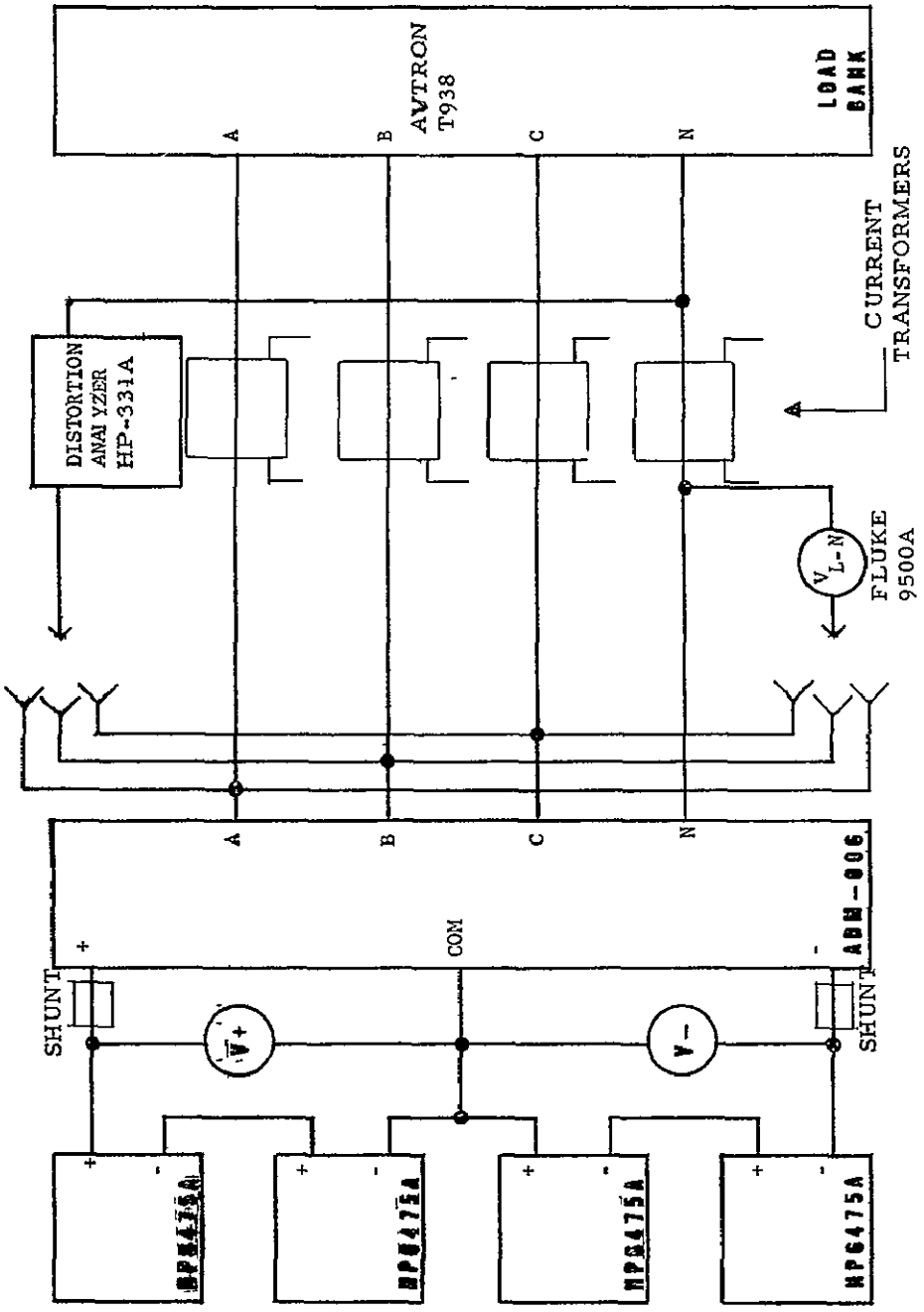

Figure 1 Test Connections

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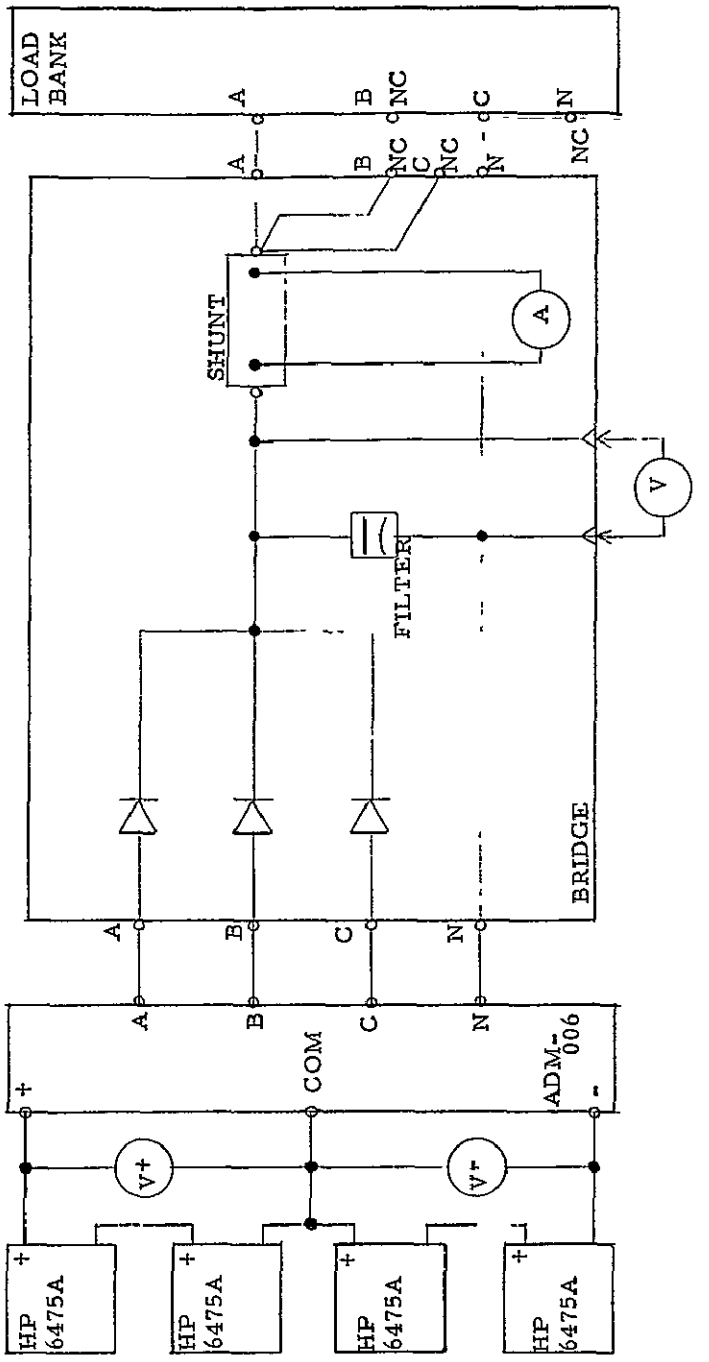

NOTE: NC = NO CONNECTION

FIGURE 2. HALF-WAVE RECTIFIER

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MSFC FORM 422 8 (VERTICAL) (NOVEMBER 1962) CONTINUATION SHEET

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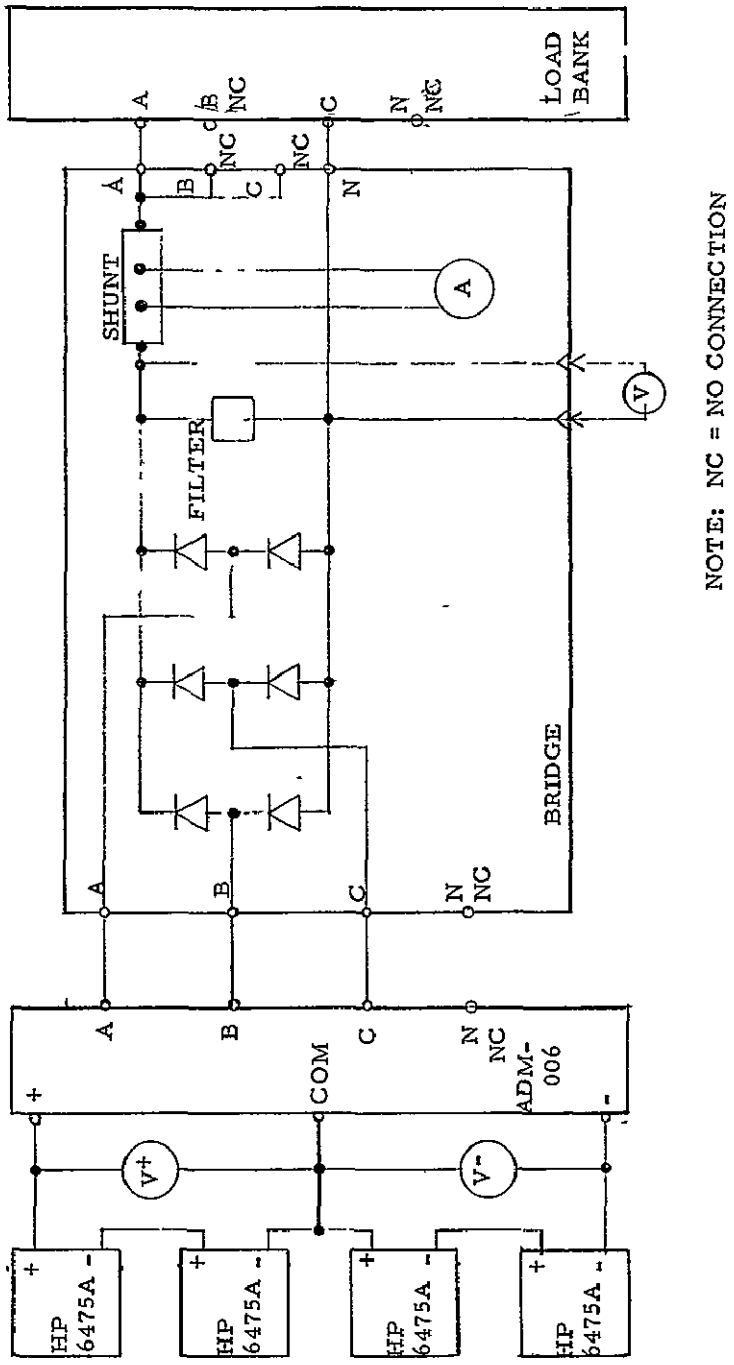

NOTE: NC = NO CONNECTION

FIGURE 3. FULL-WAVE RECTIFIER

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MSFC FORM 422-8 (VERTICAL) (NOVEMBER 1962) CONTINUATION SHEET

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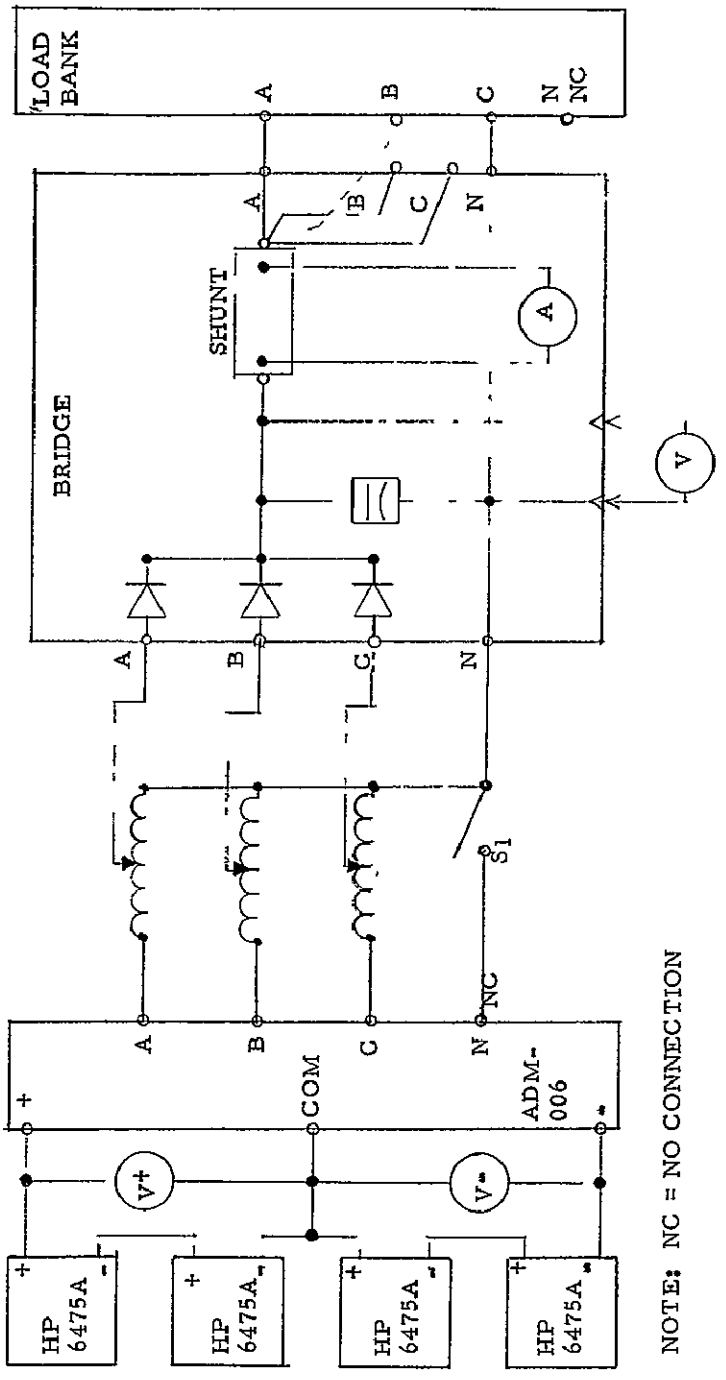

NOTE: NC = NO CONNECTION

FIGURE 4. TRANSFORMER RECTIFIER

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MSFC FORM 422-B (VERTICAL) (NOVEMBER 1962) CONTINUATION SHEET

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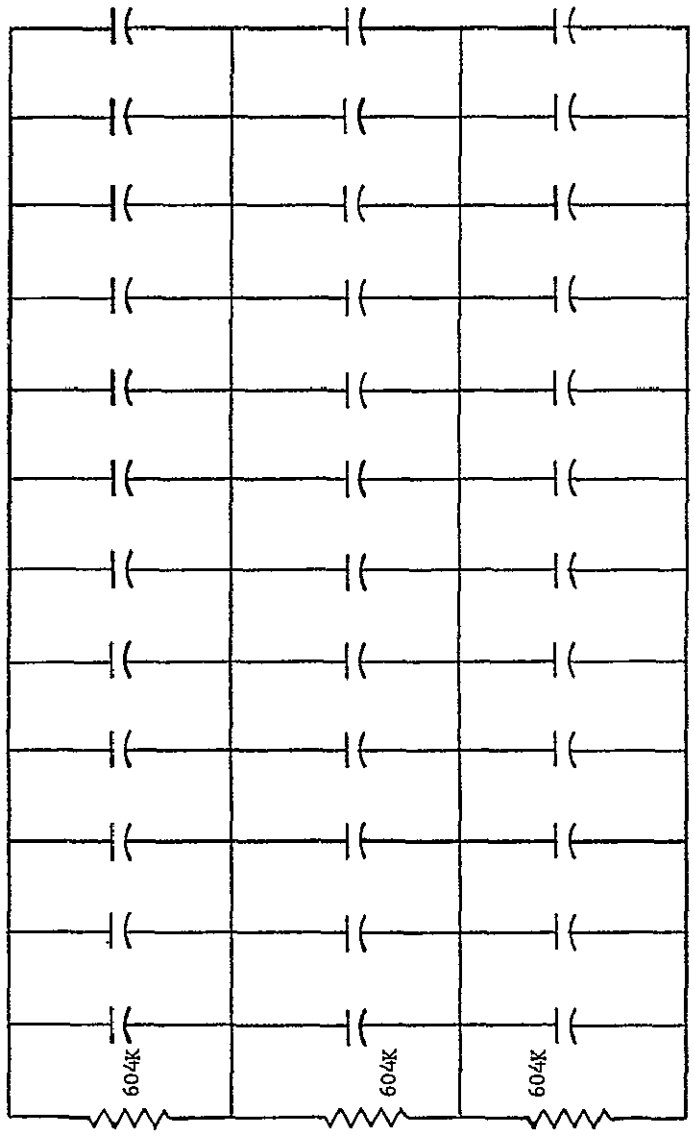

Note All capacitors will be 480 f, 125 V

Figure 5 Filter for rectifier load tests

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Table I Rated Output Power Tests.

I	II	III	IV	V
Phase A	5 KW	5 KW	8 KW	8 KW
Phase B	5 KW	5 KW	8 KW	8 KW
Phase C	5 KW	5 KW	8 KW	4 KW
(nominal)				
V_+ to Com	+ 142 VDC	+ 142 VDC	+ 142 VDC	+ 142 VDC
V_- to Com	- 142 VDC	- 142 VDC	- 142 VDC	- 142 VDC
(nominal)				
V_{A-N}, V_{B-N}, V_{C-N} (nominal)	120 V RMS	120 V RMS	120 V RMS	120 V RMS
V_+ to Com				
V_- to Com				
(measured) I_+ / I_-	/	/	/	/
V_{A-N}				
V_{B-N}				
V_{C-N}				
(measured)				
I_A				
I_B				
I_C				
(measured)				
Load (Phase A)				
Load (Phase B)				
Load (Phase C)				
(measured)				
Total Load (measured)				

Note PF = 1.0

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Table II Rated Output Voltage Tests.

Phase B	0 0 KW	1.5 KW	3 KW	4.5 KW	5 0 KW
Balanced 3 ϕ Load	No Load	4.5 KW	9 OKW	13 5 KW	15.0KW
V_+ to Com	+ 142 VDC	+ 142 VDC	+ 142 VDC	+ 142 VDC	+ 142 VDC
V_- to Com	- 142 VDC	- 142 VDC	- 142 VDC	- 142 VDC	- 142 VDC
(nominal)					
V_{AN}, V_{BN}, V_{CN} (nominal)	120 V RMS	120 V RMS	120 V RMS	120 V RMS	120 V RMS
V_+ to Com					
V_- to Com					
(measured)					
I_+					
(measured) I_-					
V_{A-N}					
V_{B-N}					
V_{C-N}					
(measured)					
I_A					
I_B					
I_C					
(measured) I_N					
THD					

Note PF = 1.0

$$\text{Regulation (\%)} = 100 \times \frac{V_{NL} - V_{FL}}{V_{FL}} =$$

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Table III. Power Factor and Waveform Tests (Inductive Loads).

Resistive KW Per Phase	2.5 KW	3.0 KW	3.5 KW	4.0 KW	4 5 KW	5 0 KW
Inductive KVAR Per Phase	4.33 KVAR	4 0 KVAR	3.57 KVAR	3.00 KVAR	2.18 KVAR	0 KVAR
Balanced 3Ø Load	15 KVA	15 KVA	15 KVA	15 KVA	15 KVA	15 KVA
Power Factor	0 5	0.6	0.7	0.8	0 9	1 0
V_{L-N} (nominal)	120 VRMS	120 VRMS	120 VRMS	120 VRMS	120 VRMS	120 VRMS
V+ to Common						
V- to Common						
I+ / I-						
IA / I_B / I_C						
V_{A-N}						
V_{B-N}						
V_{C-N}						
THD						

Note Total harmonic distortion shall be less than 4%

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Table IV. Power Factor and Waveform Tests (Capacitive Loads).

Resistive KW	.58 KW	.75 KW	.98 KW	1.33 KW	2.06 KW	5.0 KW
Capacitive KVAR Per Phase	1.0 KVAR	1.0 KVAR	1.0 KVAR	1.0 KVAR	1.0 KVAR	0 KVAR
Balanced 3Ø Load	3.46 KVA	3.75 KVA	4.2 KVA	5.0 KVA	6.88 KVA	15 KVA
Power Factor	0.5	0.6	0.7	0.8	0.9	1.0
V_{L-N} (nominal)	120 VRMS	120 VRMS	120 VRMS	120 VRMS	120 VRMS	120 VRMS
V+ to Common						
V- to Common						
I+ / I-	/	/	/	/	/	/
V_{A-N}						
V_{B-N}						
V_{C-N}						
THD						
I_A / I_B / I_C	/ /	/ /	/ /	/ /	/ /	/ /

Note Total harmonic distortion shall be less than 4%.

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Table V. Low Input Voltage Tests.

Input, Voltage	± 115 VDC		± 90 VDC	
Power factor	1.0	0.6	1.0	0 6
Balanced 3Ø Load	15 KVA	15 KVA	15 KVA	15 KVA
V+ to Com				
V- to Com				
V_{AN}				
V_{BN}				
V_{CN}				
I_+				
I_-				
I_A				
I_B				
I_C / I_N	/	/	/	/
THD				

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Table VI. Rectifier Load Tests.

	Half Wave	Full Wave	Transformer Rectifier
V_+ to Com			
V_- to Com			
I_+			
I_-			
I_A			
I_B			
I_C / I_N			
V_{out} DC			
I_{out} DC			
Output Ripple			
V_A / THD	/	/	/

Note Output ripple shall be measured with an oscilloscope (Tektronix Type 549 or equivalent)

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APPROVAL

EVALUATION OF A HIGH POWER INVERTER FOR POTENTIAL SPACE APPLICATIONS

By Buddy V. Guynes and John R. Lanier, Jr.

The information in this report has been reviewed for security classification. The report, in its entirety, has been determined to be unclassified and contains no information concerning Department of Defense or Atomic Energy Commission programs.

This document has also been reviewed and approved for technical accuracy.

for JIMMY L. MILLER
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